



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,065	01/29/2004	Toshiharu Furukawa	ROC920030268US1	5663
30206	7590	03/29/2006		
IBM CORPORATION ROCHESTER IP LAW DEPT. 917 3605 HIGHWAY 52 NORTH ROCHESTER, MN 55901-7829				
			EXAMINER NADAV, ORI	
			ART UNIT 2811	PAPER NUMBER

DATE MAILED: 03/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/767,065	FURUKAWA ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 06 March 2006.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-6, 8-10 and 25-28 is/are pending in the application.

 4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-6, 8-10 and 25-28 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892) 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>3/1/06, 3/6/06</u>	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 6) <input type="checkbox"/> Other: _____
---	--

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-6 and 8-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support in the disclosure as filed for a channel region having a vertical dimension approximately equal to a length of said at least one semiconducting nanotube and to the length of said gate electrode, as recited in claim 1, because the length of said at least one semiconducting nanotube and the length of said gate electrode are not approximately equal.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-6 and 8-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of channel region having a vertical dimension approximately equal to a length of said at least one

Art Unit: 2811

semiconducting nanotube and said gate electrode having a vertical dimension approximately equal to a length of said channel region of said at least one semiconducting nanotube, as recited in claim 1, are unclear as to how a channel region can be formed at the tip 16 of said at least one semiconducting nanotube.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 25-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Jin et al. (6,250,984).

Jin et al. teach in figure 9 and related text a semiconductor device structure, comprising:
a substrate 105;
an electrically conductive first plate 104 disposed on said substrate,
an electrically conductive second plate 100A disposed vertically above said first plate;
and
at least one nanotube having an end electrically coupled with said first plate for increasing an effective area of said first plate,; and
a dielectric layer 101A coating said length of said at least one nanotube such that said at least one nunotube is electrically isolated from said second plate,

wherein said at least one nanotube has a conducting molecular structure,
wherein said at least one nanotube has a semiconducting molecular structure,
and
wherein said dielectric layer defines a coating that encases said at least one
nanotube.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all
obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-6 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable
over Farnworth et al. (6,858,891).

Regarding claim 1, Farnworth et al. teach in figure 1 and related text a vertical
semiconductor device structure, comprising:

a substrate 12 defining a substantially horizontal plane;

a source region 17;

a drain region 21;

a gate electrode 19 disposed on said substrate and being electrically insulated
therefrom, said gate electrode positioned vertically between said source and drain
regions; and

Art Unit: 2811

at least one semiconducting nanotube 22 including a first end electrically coupled with said source region, a second end electrically coupled with said drain region, and a channel region extending vertically through said gate electrode between said source and drain regions, said channel region being electrically insulated from said gate electrode,

said channel region having a vertical dimension approximately equal to a length of said at least one semiconducting nanotube (see column 3, lines 55-56 and column 7, lines 41-42).

Farnworth et al. do not state that said gate electrode has a vertical dimension approximately equal to a length of said channel region of said at least one semiconducting nanotube.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a gate electrode having a vertical dimension approximately equal to a length of said channel region of said at least one semiconducting nanotube in Farnworth et al.'s device in order to optimize the device characteristics.

Regarding claims 4-6, 8 and 10, Farnworth et al. teach in figure 1 and related text an insulating layer disposed between said drain and said gate electrode for electrically isolating said drain from said gate electrode, an insulating layer disposed between said source and said gate electrode for electrically isolating said source from said gate electrode, wherein said at least one semiconducting nanotube is composed of arranged carbon atoms, wherein said at least one semiconducting nanotube defines a channel

Art Unit: 2811

region of a field effect transistor having a channel along which current flow is regulated by application of a control voltage to said gate electrode, wherein said at least one semiconducting nanotube is oriented substantially perpendicular to said horizontal plane, and wherein said gate dielectric is disposed on said at least one semiconducting nanotube.

Regarding claim 9, Farnworth et al. teach in figure 1 substantially the entire claimed structure, as applied to claim 1 above, except a plurality of semiconducting nanotubes extending vertically through said gate electrode. Farnworth et al. teach in figure 2 a plurality of semiconducting nanotubes 22 extending vertically through said gate electrode. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a plurality of semiconducting nanotubes extending vertically through said gate electrode in Farnworth et al.'s device in order to use the device in an practical application which requires plurality of nanotubes.

Regarding claims 2-3, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the source and drain of a catalyst material effective for growing said at least one semiconducting nanotube in Farnworth et al.'s device in order to simplify the processing steps of making the device.

Note that the process limitations of forming the source and drain of a catalyst material effective for growing said at least one semiconducting nanotube, would not carry

Art Unit: 2811

patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Response to Arguments

Applicant argues that Farnworth et al. do not teach a channel region having a vertical dimension approximately equal to a length of said at least one semiconducting nanotube.

Farnworth et al. clearly state in column 3, lines 55-56 and column 7, lines 41-42 that the nanotube acts as the channel region. Therefore, Farnworth et al. teach a channel region having a vertical dimension approximately equal to a length of said at least one semiconducting nanotube, as claimed.

Applicant argues that Jin et al. do not teach a dielectric layer coating said length of said at least one nanotube.

Jin et al. teach a dielectric layer 101A formed around said length of said at least one nanotube. Therefore, Jin et al. teach a dielectric layer 101A coating said length of said at least one nanotube, as claimed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Application/Control Number: 10/767,065
Art Unit: 2811

Page 9

A handwritten signature in black ink, appearing to read 'Ori Nadav', with a stylized, cursive script.

O.N.
3/23/06

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800